ABSTRACT OF THE DISCLOSURE

A semiconductor device includes a base P region, a source N^+ region, and a drain N^+ region formed in a surface layer portion on a principal surface in an N^- silicon layer. In the surface layer portion on the principal surface, an N well region is formed deeper than the drain N^+ region in a region including the drain N^+ region and is in contact with the base P region. A trench is formed so as to penetrate the base P region in a direction toward the drain N^+ region from the source N^+ region as a planar structure. A gate electrode is formed via a gate insulating film in the inside of the trench.